Listing of the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

Claims 1-15. (Canceled).

16. (Previously Presented) A method for the production of a bipolar transistor comprising a highly doped extrinsic base, wherein the method comprises the steps of:

providing a base layer on a semiconductor substrate;

depositing a dielectric layer in weakly doped or undoped fashion on the base layer;

applying an implantation mask and patterning in such a way that an opening remains in a region provided for a later extrinsic base;

introducing BF_2 as a dopant of a first conductivity type into the dielectric layer after the application of the mask; and

indiffusing, in a controlled thermal step, the dopant into the semiconductor substrate from the dielectric layer, an extrinsic base doped in low-resistance fashion arising.

17. (Previously Presented) The method as claimed in claim 16, in which an oxide layer is deposited as the dielectric layer (DS).

18. (Previously Presented) The method as claimed in claim 16, in which an emitter window is opened in the dielectric layer.

19. (Previously Presented) The method as claimed in claim 18, in which before the dopant is introduced into the dielectric layer, the emitter is produced by application and patterning of a polycrystalline emitter layer doped with a dopant of the second conductivity type above the emitter window.

20. (Previously Presented) The method as claimed in claim 19, in which the emitter layer is patterned by means of a photopatterned resist mask that remains on the emitter and is later used as an implantation mask for the implantation of the dopant into the dielectric layer.

21. (Previously Presented) The method as claimed in claim 16, in which, for the production of the semiconductor substrate, in a semiconductor wafer doped with a dopant of the second conductivity type, active transistor regions are defined and are electrically insulated by oxide regions; and

in which a base layer weakly doped with a dopant of the first conductivity type is grown epitaxially over the whole area.

22. (Previously Presented) The method as claimed in claim 16, in which a buried collector layer doped with a dopant of the second conductivity type is produced by implantation in the semiconductor wafer in the active transistor region, said collector layer serving for electrical connection of the collector.

23. (Previously Presented) The method as claimed in claim 16, in which BF_2 is implanted for the introduction of the dopant into the dielectric layer.

24. (Previously Presented) The method as claimed in claim 16, in which BF_2 can be indiffused into the dielectric layer from the gas phase.

25. (Previously Presented) The method as claimed in claim 19, in which the emitter layer is doped with arsenic, in which, during the indiffusion of the dopant into the base layer (BS), arsenic also indiffuses into a surface region of the base layer (BS) from the emitter (E).

26. (Previously Presented) The method as claimed in claim 19, in which the dielectric layer is removed after the patterning of the emitter layer and after the outdiffusion of the dopant in uncovered regions by etching.

27. (Previously Presented) The method as claimed in claim 19, further comprising the steps of:

providing an n-doped semiconductor;

growing a p-doped base layer epitaxially on the semiconductor wafer over the whole area;

applying a dielectric layer in weakly doped or undoped fashion on the base layer;

opening an emitter window in the dielectric layer;

producing the emitter by application and patterning of an As-doped polycrystalline emitter layer above the emitter window;

introducing BF_2 as the dopant into the dielectric layer with the aid of an implantation mask; and

in a controlled thermal step, indiffusing boron from the dielectric layer into the base layer in the region of the extrinsic base, the latter acquiring low resistance, and simultaneously indiffusing arsenic into an upper region of the base layer from the emitter through the emitter window.

28. (Previously Presented) The method as claimed in claim 27, in which a photomask applied over an oxide layer over the emitter is used as the implantation mask, said photomask already having been used beforehand for the patterning of the emitter layer.

29. (Previously Presented) The method as claimed in claim 27, in which the collector connection is effected via an n^+-doped buried layer, and in which, over the emitter and in the region of the extrinsic base, the respective semiconductor is uncovered and metallic contacts are produced above the latter.